REMARKS

This Amendment is filed in response to the Office Action dated July 12, 2005, which has a shortened statutory period set to expire October 12, 2005.

Applicants Overcome The 112 Rejection

The Office Action states that the word "system" recited in Claims 23-32 and 39-44 renders the claims ambiguous because a system is similar to a method and/or apparatus. Applicants respectfully traverse this rejection.

Figure 1 illustrates a computer system forming a part of a system in accordance with one embodiment of the present claimed invention. Specification, page 8, lines 4-6. As shown in Figure 1, computer system 112 can include a central processor 101 for processing information and instructions. Specification, page 12, lines 1-5. Applicants submit that describing instructions as steps (thereby implementing a method) is common and does not render the claims ambiguous.

Based on the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 23-32 and 39-44 under U.S.C. 112, second paragraph.

Applicants Overcome The 103 Rejections

Claim 1 recites in part:

determining a maximum forward delay sum for each node;
determining a safe delay period for each of said output nodes;
removing timing checks from those output nodes for which the maximum forward delay sum is less than the safe delay period;
determining a minimum reverse delay difference for each of a portion of said nodes;
identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward delay sum;

setting the delays for the identified nodes to zero; and

performing dynamic timing simulation.

Applicants respectfully traverse the rejection of Claim 1 as being obvious over Pillage in view of Gamal. Specifically, in the rejection of Claim 1 (and other claims), the Office Action cites column 7, lines 20-26, and column 12, lines 5-10 of Pillage as well as column 2, lines 10-13, column 3, lines 35-40, column 7, lines 35-46, 60-65, and column 8, lines 5-8 of Gamal. For ease of reference, these passages are included below.

It will be understood by those having skill in the art that the entire microelectronic circuit may be described in terms of a "netlist" which defines component types, component values and component interconnects for all of the components of the integrated circuit. The netlist is then parsed, using techniques well known to those skilled in the art, to separate the interconnect elements from the active elements. Pillage, column 7, lines 19-26.

Referring now to TABLE 3, identification of the fundamental loop associated with any specified link in the graph begins by initiating a backward and forward traversal of the spanning tree starting at each of the link nodes. The traversal direction is always towards the ground via the inward branch and the traversal alternates between the two prongs. Pillage, column 12, lines 5-10.

The library 10 is usually provided by the ASIC vendoe, and typically includes macrocells such as logic gates, sequential logic functions, adders, counters, multiplexers, and latches among other standard functions. Gamal, column 2, lines 10-13.

The motivation for the present invention is to address the above problems by developing an IC design methodology where the IC can be manufactured under a number of different fabrication processes, where the designer does not perform a separate simulation and development cycle for each process, and where the IC die size is optimized for each process. This

methodology will reduce the product development and manufacturing costs as well as get the product to market faster. Gamal, column 3, lines 33-41.

In the preferred embodiment, the designer simulates the synthesized generic digital circuit by running a simulation program that uses back annotated timing data in SDF (Standard Delay Format). The SDF data is produced by a back-annotation program that computes the macrocell timing arcs (input pin to output pin delays) using the performance characteristics from the process specific libraries 16. The back-annotation program selects the maximum delay, the minimum delay, and the average delay for each timing arc over all the processes in the club. The simulation program thus uses the back-annotated data to emulate the overall digital circuit under maximum, minimum, or average delay conditions. For all conditions, these delays constitute the estimated timing of the circuit before placement and routing. Gamal, column 7, lines 32-46.

When placing and routing generic macrocells, a generic base array must be used. The virtual routing grid 20 for the generic base array is defined by the generic base cell alignment grid, as shown in FIGS. 4A and 5A. The generic base cell alignment grid is chosen so that generic design rules can be applied for automatic placement and routing tools. Gamal, column 7, lines 60-66.

In the preferred embodiment, such a program inputs the generic design rules, a description of the generic CBA library and base array, and the netlist description of the digital circuit before performing automatic placement and routing. This program attempts to optimize the placement and routing by creating only legal placements and physical connections while minimizing interconnect parasitics. Gamal, column 8, lines 3-10.

Applicants respectfully submit that these passages, taken individually or in combination, fail to disclose or suggest the recited steps of Claim 1. Applicants also traverse the characterization that any recited step is an "inherent feature

of logic functions as well as simulation". Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 1.

Claims 2-11 depend from Claim 1 and therefore are patentable for at least the reasons presented for Claim 1. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 2-11.

Moreover, Applicants submit that the passages cited with respect to Claims 2, 7, 8, 9, 10, and 11 do not disclose or suggest the limitations in those claims. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 2, 7, 8, 9, 10, and 11.

Claim 12 recites in part:

> determining a maximum forward delay sum for each node;
> determining a safe delay period for each of said output nodes;
> removing timing checks from those output nodes for which the maximum forward delay sum is less than the safe delay period;
> determining a minimum reverse delay difference for each of a portion of said nodes;
> identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward delay sum;
> setting the delays for the identified nodes to zero; and
> compiling the logic simulator.

Notably, the Office Action cites the same passages as those cited for Claim 1. Applicants again traverse the characterization that any recited step is an "inherent feature of logic functions as well as simulation". Therefore, Applicants submit that Claim 12 is patentable for substantially the same reasons presented for Claim 1. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 12.

Claims 13-22 depend from Claim 12 and therefore are patentable for at least the reasons presented for Claim 12. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 13-22.

Moreover, Applicants submit that the passages cited with respect to Claims 13, 18, 19, 20, 21, and 22 do not disclose or suggest the limitations in those claims. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 13, 18, 19, 20, 21, and 22.

Claim 23 recites in part:

> determining a maximum forward delay sum for each node;
> determining a safe delay period for each of said output nodes;
> removing timing checks from those output nodes for which the maximum forward delay sum is less than the safe delay period;
> determining a minimum reverse delay difference for each of said interior nodes and said input nodes;
> identifying the nodes for which the minimum reverse delay difference is greater than the maximum forward delay sum;
> setting the delays for the identified nodes to zero; and
> compiling the logic simulator.

Once again, the Office Action cites the same passages as those cited for Claim 1. Applicants again traverse the characterization that any recited step is an "inherent feature of logic functions as well as simulation". Therefore, Applicants submit that Claim 23 is patentable for substantially the same reasons presented for Claim 1. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 23.

Claims 24-32 depend from Claim 23 and therefore are patentable for at least the reasons presented for Claim 23.

Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 24-32.

Moreover, Applicants submit that the passages cited with respect to Claims 24, 29, 30, 31, and 32 do not disclose or suggest the limitations in those claims. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 24, 29, 30, 31, and 32.

Claim 33 recites in part:

> b) removing timing checks on sequential elements indicated as exempt from timing checks based on said delay information;
> c) assigning zero delay to certain gates based on said delay information; and
> d) performing dynamic simulation on said netlist, wherein said dynamic simulation enhances performance by:
> performing cycle based simulation with respect to gates having assigned thereto zero delay as indicated by c); and
> skipping timing checks for exempt sequential elements as indicated by b).

Applicants respectfully submit that the cited passages used in this rejection, taken individually or in combination, fail to disclose or suggest these steps. Applicants also traverse the characterization that any recited step is an "inherent feature of logic functions as well as simulation". Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 33.

Claims 34-38 depend from Claim 33 and therefore are patentable for at least the reasons presented for Claim 33. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 34-38.

Moreover, Applicants submit that the passages cited with respect to Claims 35, 36, 37, and 38 do not disclose or suggest the limitations in those claims. Therefore, Applicants request

further reconsideration and withdrawal of the rejection of Claims 35, 36, 37, and 38.

Claim 39 recites in part:

    b) removing timing checks on sequential elements indicated as exempt from timing checks based on said delay information;
    c) assigning zero delay to certain gates based on said delay information; and
    d) performing dynamic simulation on said netlist, wherein said dynamic simulation enhances performance by:
    performing cycle based simulation with respect to gates having assigned thereto zero delay as indicated by c); and
    skipping timing checks for exempt sequential elements as indicated by b).

Notably, the Office Action cites the same passages as those cited for Claim 33. Applicants again traverse the characterization that any recited step is an "inherent feature of logic functions as well as simulation". Therefore, Applicants submit that Claim 39 is patentable for substantially the same reasons presented for Claim 33. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 39.

Claims 40-44 depend from Claim 39 and therefore are patentable for at least the reasons presented for Claim 39. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 40-44.

Moreover, Applicants submit that the passages cited with respect to Claims 41, 42, 43, and 44 do not disclose or suggest the limitations in those claims. Therefore, Applicants request further reconsideration and withdrawal of the rejection of Claims 41, 42, 43, and 44.

(SN: 10/015,180)

CONCLUSION

Claims 1-44 are pending in the present Application. Applicants respectfully request allowance of these claims.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 7, 2005.

10/7/2005
Date

Signature: Rebecca A. Baumann

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